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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,492	03/01/2004	Patrick Morrow	P17817	1866

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INTEL CORPORATION
c/o INTELLEVATE, LLC
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
POMPEY, RON EVERETT	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,492	MORROW ET AL.	
	Examiner	Art Unit	
	Ron E. Pompey	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-32* is/are pending in the application.

4a) Of the above claim(s) *18 and 24-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-17,19-21,23 and 27-32* is/are rejected.

7)☒ Claim(s) *22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 15, 27-28, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (USPGPub 2002/0158318).

Chen discloses the limitations of:

sealing a device, the device comprising:

a substrate with a top surface ([0030]);

a first integrated circuit die (230, fig. 4) above the substrate and spaced apart from the substrate by a first distance (the diameter of solder balls attached to contacts 246) to form a first volume between the substrate and the first integrated circuit die, the first integrated circuit die having a bottom surface closer to the substrate and a top surface further from the substrate and a plurality of microelectronic devices (fig. 5, because there is no mention of forming two microelectronic devices on the upper surface of die 230 in figure 5 it is taken that one or more microelectronic device can be place on die 230 during any of the different embodiments);

a first plurality of connectors (solder balls attached to contacts 246, fig. 4) extending from the top surface of the substrate to the bottom surface of the first

integrated circuit die and forming an electrical connection between the substrate and the bottom surface of the first integrated circuit;

a second integrated circuit die (210, fig. 4) above the first integrated circuit die and spaced apart from the first integrated circuit die by a second distance to form a second volume (240a, fig. 4) between the first integrated circuit die and the second integrated circuit die, the second integrated circuit die having a bottom surface closer to the first integrated circuit die and a top surface further from the first integrated circuit die and a plurality of microelectronic devices (210, fig. 4);

a second plurality of connectors (272, fig. 4) extending from the first integrated circuit die to the second integrated circuit die;

wherein sealing (270, fig. 4) the device comprises substantially sealing volume between the first and second integrated circuit dies from a surrounding environment (note: a chip, which 230 and 210 are, contains multiple microelectronic devices);

wherein the first plurality of connectors does not extend substantially beyond the top surface of the substrate or the bottom surface of the first integrated circuit;

wherein the second plurality of connectors does not extend substantially beyond the top surface of the first integrated circuit or the bottom surface of the second integrated circuit;.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16-17,19-21, 23, 29 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (USPGPub 2002/0158318) as applied to claim 15 and 30 above, in view of Beyne et al. (US 6566745) and in further view of Jiang (US 677268) and Lee (US 6613606).

5. Chen reads on the claims as applied above, but does not disclose the claimed limitation(s) of:

wherein formation of device comprises: fabricating the first integrated circuit die, the fabricated first integrated circuit die having a first set of first portions of the second plurality of connectors;

fabricating the second integrated circuit die, the fabricated second integrated circuit die having a second set of second portions of the second plurality of connectors;

singulating the first integrated circuit die from a first wafer comprising a plurality of dies;

singulating the second integrated circuit die from a second wafer comprising a plurality of dies;

and

bonding the first set of first portions to the second set of second portions to connect the first integrated circuit die to the second integrated circuit die;

wherein the device is sealed after the first and second integrated circuit dies have been singulated from the first and second wafers;

wherein the device is sealed by a layer of underfill material and the layer of underfill material comprises filler particles having an average diameter greater than the second distance between the first integrated circuit die and the second integrated circuit die;

wherein the first distance between the substrate and the first integrated circuit die is in a range from about 75 microns to about 100 microns, and the second distance between the first integrated circuit die and the second integrated circuit die is in a range from about 100 nanometers to about 200 nanometers;

wherein sealing the device comprises applying a layer of underfill material extending from the substrate to the second integrated circuit die;

wherein the device is sealed by a layer of underfill material and the second volume between the first integrated circuit die and the second integrated circuit die and around the second plurality of connectors is substantially free of the underfill material;

wherein sealing the device comprises applying a layer of material extending from the first integrated circuit die to the second integrated circuit die.

wherein sealing the device comprises applying a single layer of underfill material extending from the substrate to the second integrated circuit die, the layer of underfill material being in contact with both the first and second integrated circuit dies.

However,

a. Beyne discloses the above claimed limitations regarding:

forming singulated dies (fig. 5C) with connectors formed on each die;

wherein the connectors are bonded together (fig. 5D,E) to connect the two dies in column(s) 7, line(s) 43-50.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Beyne with Chen, because the connectors help provide a hermetic cavity.

b. Jiang discloses the above claimed limitations regarding:

an underfill material (258, fig. 20) with filler particles (266, fig. 20) having an average diameter greater than the distance between the first and second integrated circuit die column(s) 3, line(s) 22-45.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Jiang with Chen and Beyne, because the filler particles will increase the hermetic seal on the cavity of Chen and Beyyne.

c. Lee discloses the above claimed limitations regarding:

sealing the device with a layer of underfill material (53, fig. 11) that extends from the substrate (50, fig. 11) to the second integrated circuit die column(s) 9, line(s) 32-40.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Lee with Chen and Beyne, because the underfill material that extends from the substrate to the second integrated circuit die improves the stability of package.

Neither Chen, Beyne, Jiang nor Lee, disclose the distance range between the substrate and the first integrated circuit die or the first integrated circuit die and the second integrated circuit die. However, since it has been held that where the general

conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the connectors to these ranges, because the ranges of distances are typical ranges to form connectors.

Also, Chen discloses the limitations of wherein sealing the device comprises applying a layer of material extending form the first integrated circuit die to the second integrated circuit die. However, because this limitation was dependent on a claim that was not disclosed in Chen it was not rejected in the 102 rejection above.

Allowable Subject Matter

2. Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, either singly or in combination, fails to disclose the limitations of:

wherein the device is sealed by a layer of underfill material and the second volume between the first integrated circuit die and the second integrated circuit die and around the second plurality of connectors is substantially free of the underfill material. None of the prior art of record describes, written or drawing, wherein the underfill does not fill in volume around or not touch the second plurality of connectors.

Response to Arguments

4. Applicant's arguments with respect to claims 15-17, 19-23 and 27-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ron Pompey
AU: 2812
September 1, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER